MODELING AND PERFORMANCE OF A SUB-NANOSECOND HIGH ISOLATION DC-18 GHz MONOLITHIC SPST WITH DRIVER

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ABSTRACT

The design, computed performance using linear and non linear modeling and experimental results of a DC-18 GHz high-isolation ultra-fast monolithic SPST switch with driver are presented. A non linear modeling of the SPST and of the driver was carried out in order to predict the switching time of the overall circuit. The monolithic SPST design uses GaAs FETs and the driver uses GaAs devices in order to reach a very short switching time. Insertion loss less than 2.4 dB, a typical isolation of 50 dB and a switching time less than 1 ns, driver included, were obtained. The validity of the non linear-models used were demonstrated by the good agreement obtained between the simulated and the measured performance.

INTRODUCTION

Modern EW systems need fast microwave switching circuits in order to perform amplitude modulation with high modulation frequency. The switching time of a single-pole single-throw (SPST) design, using GaAs FETs as the microwave switching elements, depends on the SPST on the driver itself, and on the coupling of the driver with the FETs. In order to optimize the design for ultra-fast switching time it becomes necessary to predict it and to control the linear and non-linear performance of the design ; in particular the designer must consider the isolation and the time response of the circuit. To predict the time response of the switch a non-linear modeling of the SPST and of the driver circuit were carried out. This paper presents the non-linear modeling and simulations ; a comparison between the theoretical and measured performance is presented too. The microwave part is a monolithic DC-18 GHz reflective SPST using eight 0.5 µm GaAs FETs. The driver circuit uses a GaAs logical gate in order to reach a very short time response. From DC to 18 GHz the SPST exhibits less than 2.4 dB insertion loss and typically 50 dB of isolation ; the switching time is less than 1 ns, including the driver.

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The monolithic SPST was developped in THOMSON-CSF/RCM using THOMSON-CSF/DAG foundry ; the driver uses GaAs devices provided by THOMSON-CSF/DAG.

SPST DESIGN AND MODELING

The scheme of the monolithic SPST is shown in figure 1 ; it is composed of eight GaAs FETs in a shunt configuration. Each FET exhibits a 0.5 µm gate lenght and a 2x75 µm gate width.

A single control voltage is used to switch the FETs from a high impedance state to a low impedance state. The control is applied to the gates of the FETs through a high value resistance (Rc). The number of transistors and the value of the command resistance (Rc) was chosen in order to obtain the required isolation (50 dB typical) with less than 2.5 dB insertion loss at 18 GHz. The choice of this design was compatible with the required switching time. A photography of the monolithic SPST is shown in figure 2 ; the dimensions of the chip are 2.5 mm x 1 mm x 0.1 mm. The SPST model uses the FET model shown in figure 3. The main non-linear elements of this model are the gate to source capacitance (C_{GS}), the gate to drain capacitance (C_{GD}) and the drain to source

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resistance (R_{DS}) ; these three elements depend on the gate to source voltage (V_{GS}).

For predicting the time response of the switch a modeling of these non-linear elements was carried out using measurements of the equivalent scheme shown in figure 3 for several V_{GS} values. The non-linear modeling of C_{GS}, C_{GD} and R_{DS} are shown in figures 4 to 6 where the computed responses given by the non-linear models show a good agreement with the measured ones.

DRIVER DESIGN AND MODELING

For the design of the driver circuit the aim was supply the FETs with the control signal shown in figure 7 in order to obtain an amplitude modulation at a fixed frequency of 25 MHz with the maximum isolation and with a switching time less than 1 ns. The schematic diagram of the driver is shown in figure 9. The driver uses an oscillating logical gate to produce the control signal at 25 MHz ; a serial capacitance and a paralle Schottky diode are used to set the control voltage values shown in figure 7.

The GaAs logical gate delivers a variable voltage from 1 V to 5 V and features at its output an impedance varying from a low to a high level. This is why it can be modeled by (see fig. 8) the THEVENIN generator where R_T is a function of R_{TO}, E_T, α and β ; and α are β best fit parameters (α = 2,098, β = 0,34). The Schottky diode non linear model used is shown in figure 10.

LINEAR PERFORMANCE

The measured performance is shown in figure 11. From DC to 18 GHz the insertion loss is less than 2.4 dB, the minimum isolation is 28 dB, the typical isolation is 50 dB ; the SWR is less than 2.

NON-LINEAR PERFORMANCE

♦Firstly the leakage of the modulation signal at the RF output of the SPST was simulated using the non-linear models previously described and a non-linear analysis software.

When the modulation signal is applied to the FETs the simulated modulation leakage at the RF output is represented in figures 12a and 12b ; figure 12a shows the front voltage peak and figure 12b shows the last voltage peak. Figures 13a and 13b show the corresponding measured voltages.

The modulation leakage depends on :

. the spectral composition of the modulation signal,

. the variation of the non-linear elements of the FETs with the gate to source voltage,

. the filtering characteristics of the driver and of the coupling circuits.

The predicted and measured responses are in a good agreement : the voltage peaks duration is of the order of 1 ns.

♦Secondly the rise and fall times were simulated with a 11 GHz continuous wave entering the SPST RF input. The predicted rise and fall times of the amplitude modulated RF signal are shown in figure 14a and 14b ; the corresponding measured responses are shown in figure 15a and 15b ; figure 15c is an overall view of the RF output signal.

The predicted and measured responses are in a good agreement. The rise time is nearly 300 ps ; the fall time is nearly 600 ps. The rise and fall time are defined as the switching time between the minimum insertion loss state and the state where the maximum attenuation at the operating frequency is reached.

CONCLUSION

Theoretical and experimental results concerning a high isolation, subnanosecond MMIC SPST switch with driver have been presented. The DC-18 GHz switch features 2.4 dB maximum insertion loss, 50 dB typical isolation and a switching time less than 1 ns. Use of GaAs MMIC for the SPST switch and GaAs logical gate for the driver have made possible the realisation of this ultra fast high isolation switching circuit.

The good agreement between simulated and experimental results

demonstrates the validity of the non-linear models used for the SPST switch and for the driver.

To our knowledge it is the first time such an ultra fast MMIC SPST switch with driver is reported in the litterature.

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[3] C. KERMARREC, B. MAOZ and J. ODELL : Accurately model unbiased FETs for monolithic switches.

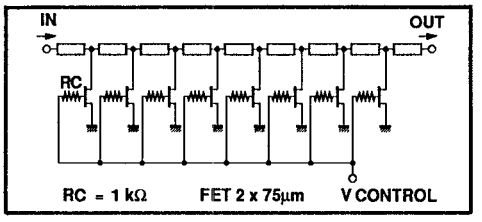

Fig 1 : SPST scheme

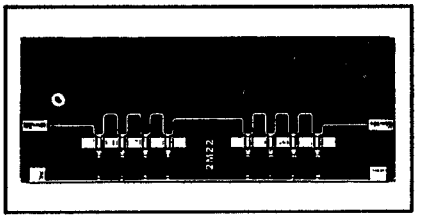

Fig 2 : DC-18 GHz monolithic SPST

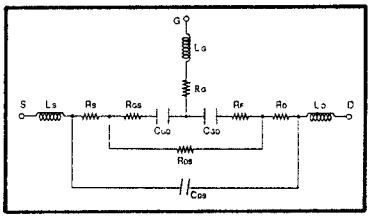

Fig 3 : FET model

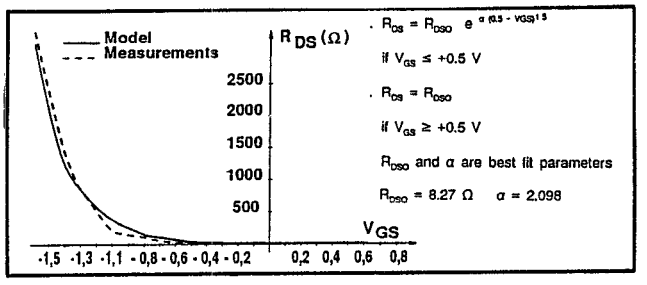

Fig 4: R_{DS} versus V_{GS}

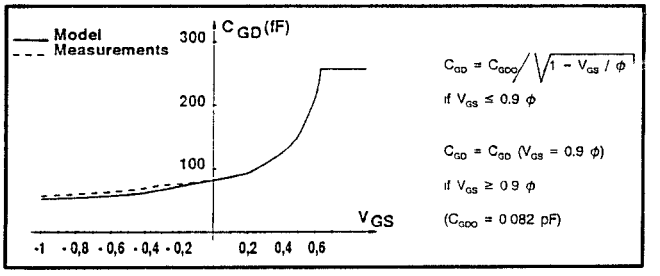

Fig 5 : C_{GD} versus V_{GS}

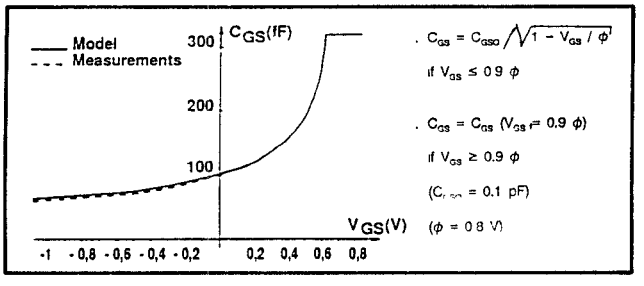

Fig 6 : C_{GS} versus V_{GS}

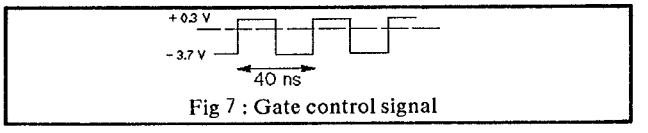

Fig 7 : Gate control signal

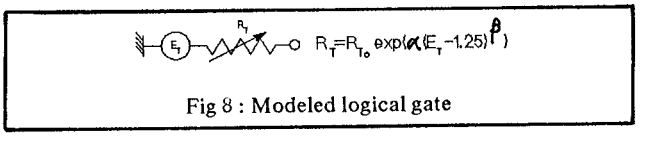

Fig 8 : Modeled logical gate

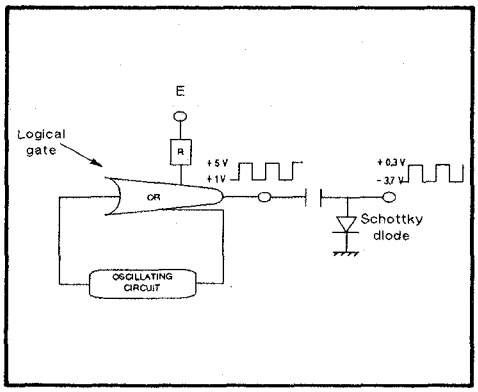

Fig 9 : Schematic diagram of the driver

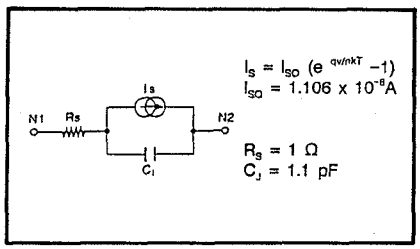

Fig 10 : Schottky diode non linear model

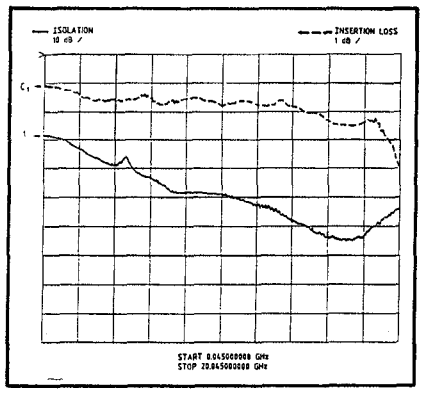

Fig 11 : Measured isolation and insertion loss

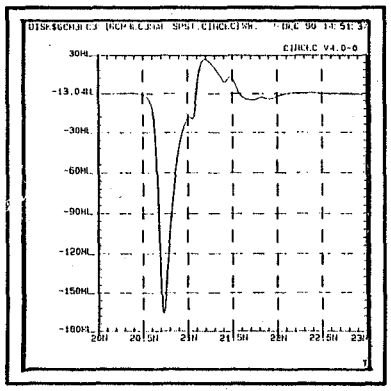

Fig 12a : Predicted front peak

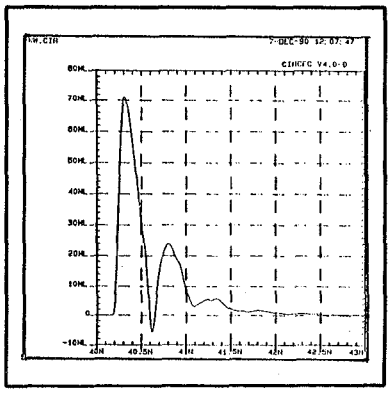

Fig 12b : Predicted last peak

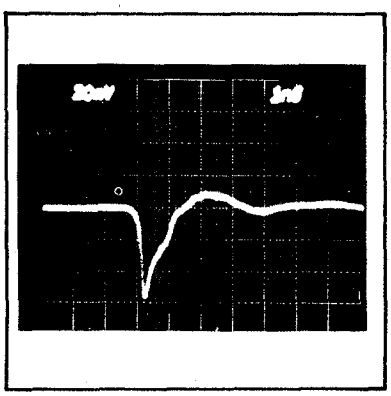

Fig 13a : Measured front peak

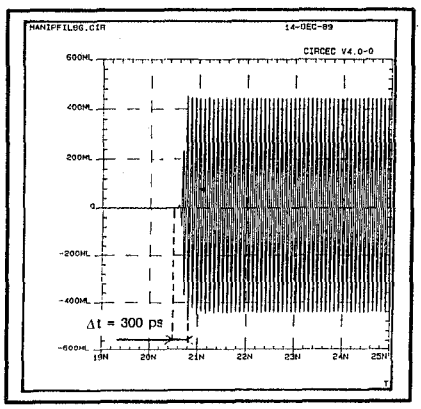

Fig 14a : Predicted rise time

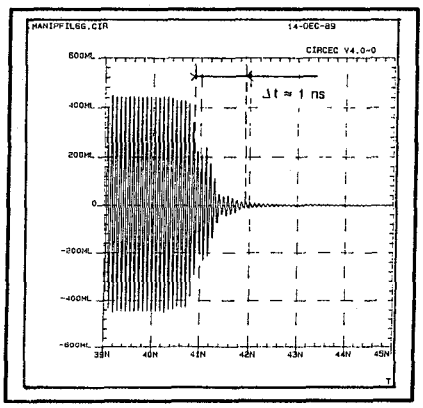

Fig 14b : Predicted fall time

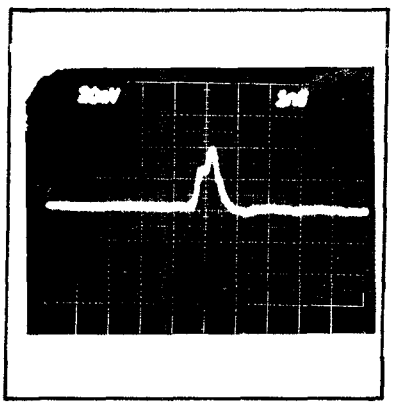

Fig 13b : Measured last peak

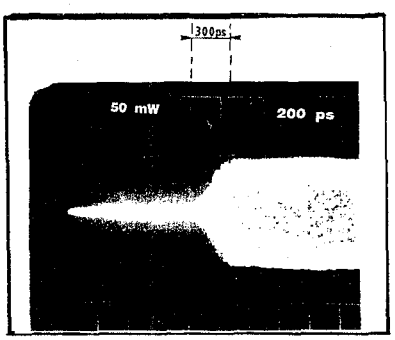

Fig 15a : Measured rise time

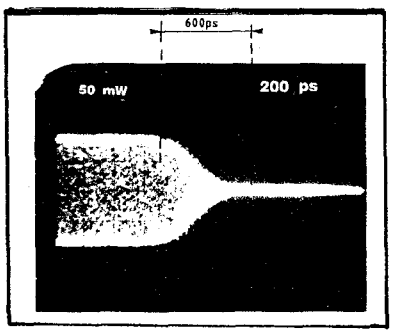

Fig 15b : Measured fall time

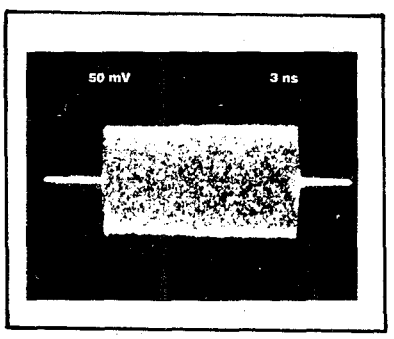

Fig 15c : Measured RF output pulse